SPERRY UNIVAC

Magnetic Tape System
Model 70-7100
Operation and Service

Mini-Computer Operations
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98A 9902 123

UNIVAC®

MAGNETIC TAPE SYSTEM

MODEL 70-7100; P/N 01P0869-000

OPERATION AND SERVICE MANUAL

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CHANGE RECORD

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Change Procedure:

When changes occur to this manual, updated pages are issued to replace the obsolete pages. On each updated page, a vertical line is drawn in the margin to flag each change and a letter is added to the page number. When the manual is revised and completely reprinted, the vertical line and page-number letter are removed.

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94A0731-000B

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DESCRIPTION

1.1 GENERAL

The SPERRY UNIVAC Model 70-7100 Magnetic Tape System is a peripheral option for the SPERRY UNIVAC 71 through 77 Computers. The 9-track magnetic tape system consists of a controller and up to four magnetic tape transports (Peripheral Equipment Corporation series 6000).

The magnetic tape controller (MTC) is a buffered interface between the I/O bus and the tape transport. The MTC accommodates up to four tape transports, but only one of these is in use at any given time.

The MTC provides:

a. Timing for response to motion instructions from the computer.

b. Timing for data flow between the computer and the tape transport.

c. Tape system status information to the computer in response to sense instruction.

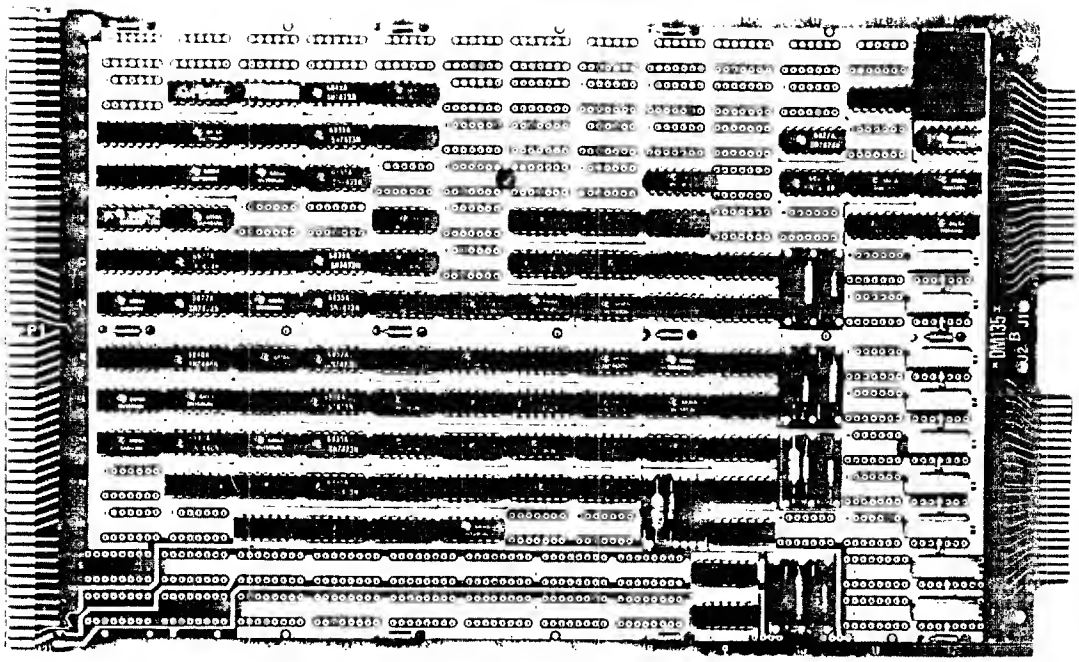
d. Data buffering to reduce the response time.

1.2 PHYSICAL DESCRIPTION

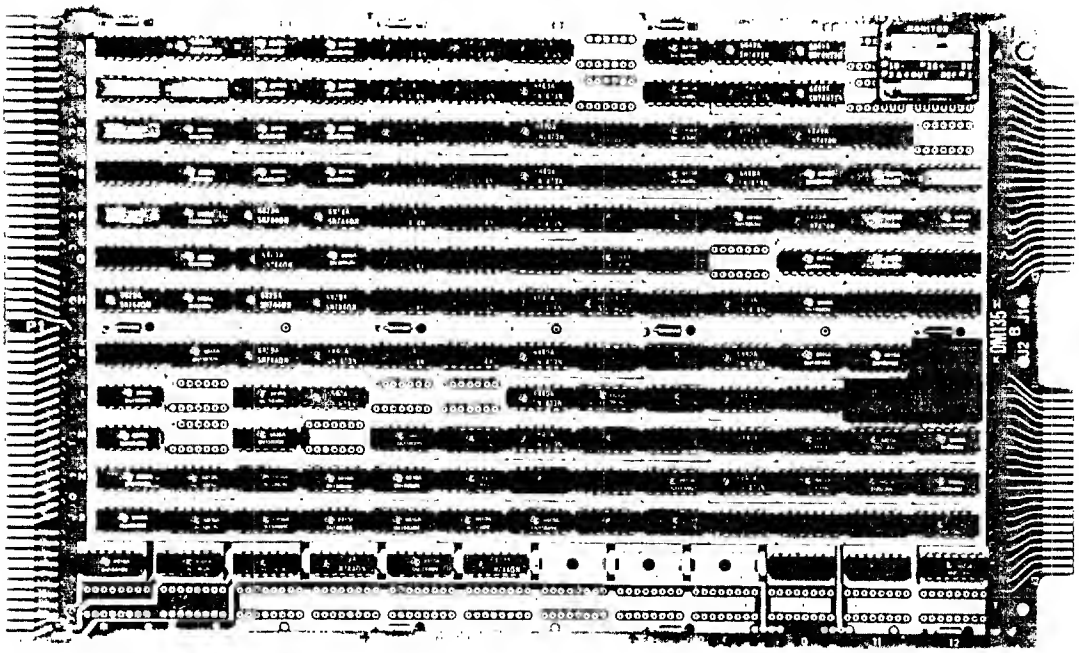
The MTC is on two wire-wrap circuit boards (figure 1-1). It contains all read/write registers and logic circuitry for the control of the tape transport.

The tape transports are in a standard nineteen-inch rack chassis.

The computer controls the MTC through the I/O cable or the optional buffer interlace controller (BIC). A transport cable carries data between the tape transport and the MTC. Figure 1-2 shows the tape system configuration.



A. Board No. 1 (Part No. 44P0232-000).



B. Board No. 2 (Part No. 44P0233-000).

FIGURE 1-1. Magnetic Tape Controller Boards (9-Track).

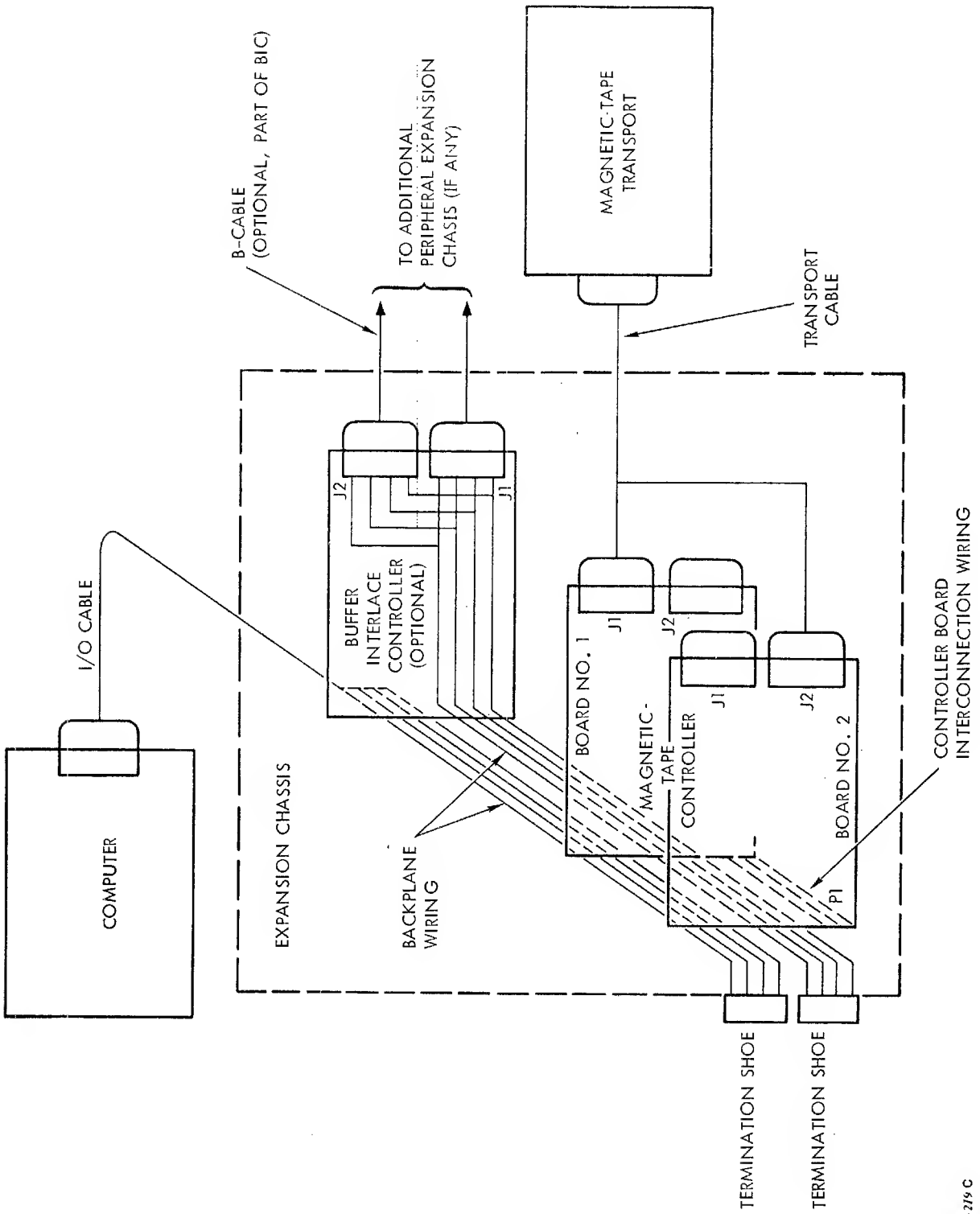


FIGURE 1-2. Tape System Configuration.

> NOTE
>
> In the text of this manual, numbers beginning with a digit other than zero are decimal numbers, numbers with a leading zero are octal, and numbers preceded by a dollar sign ($) are hexadecimal.

If the computer system contains a BIC in the same expansion chassis as the MTC, the two are connected through the backplane wiring. If the computer system contains a BIC in an expansion chassis other than that containing the MTC, the B cable of the BIC provides the connection.

If the system contains more than one tape transport, the transports are connected to the MTC in party-line configuration (figure 1-3). The program controls the selection of the one transport that can operate at any given time, but a system reset automatically selects transport No. 1.

1.3 SPECIFICATIONS

Table 1-1 lists the specifications of the MTC, and table 1-2 those of the tape transport.

Table 1-1. Magnetic-Tape Controller (Nine-Track) Specifications

Organization	Consists of a clock, drivers, receivers, and the following logic sections: instruction decoding, instruction storage, sense, read/write motion control, read/write data control, read/write data storage, and error checking.
Control	Can select one of up to four tape transports at any given time. Resetting the system automatically selects tape transport No. 1.
Size	Two 7-3/4-by-12-inch wire-wrap circuit boards.

(continued)

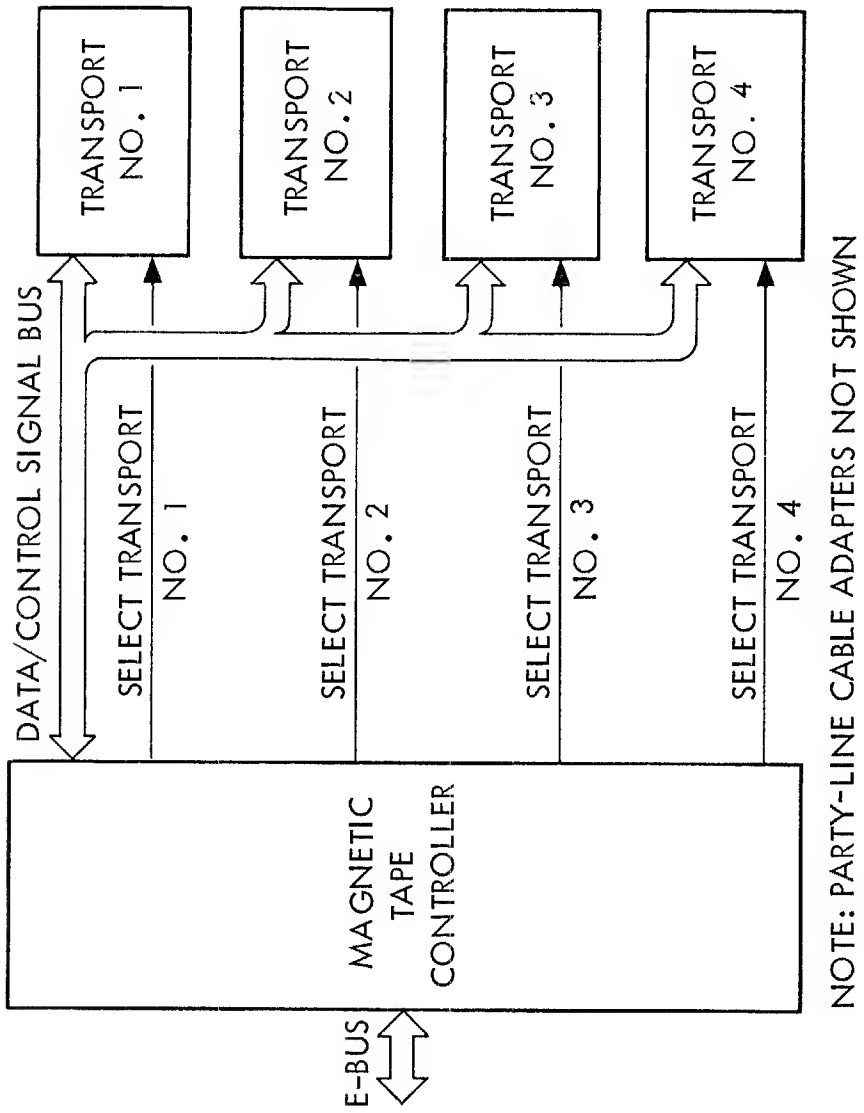


FIGURE 1-3. Tape System Party-Line Configuration

Table 1-1. Magnetic-Tape Controller (Nine-Track) Specifications (continued)

Connections	The MTC interfaces with the I/O cable through the backplane connector and with the tape transports through the tape-transport cable (20 feet maximum). The MTC boards are connected to each other by their backplane and P1 connectors. They are in adjacent card slots (figure 1-2).
Connectors	One 122-terminal card-edge connector on each card, mating with female connectors on the chassis backplane. Two 44-terminal card-edge connectors on each card, one on each card mating with a female connector on the tape-transport cable.
Data Word	Buffering is provided for two 16-bit words, each containing two 8-bit bytes.
Error Checking	During writing, cyclic redundancy check (CRC) characters and longitudinal redundancy check (LRC) characters are written for each tape record. During reading, these characters are regenerated and compared with those read. The LRC includes a parity check. Error correction is not provided.
Logic Levels:	
I/O and B Cables	Negative Logic: High: +2.8 to +3.6V dc Low: 0 to +0.5V dc
Internal	Positive Logic: High: +2.4 to +5.0V dc Low: 0 to +0.4V dc

(continued)

Table 1-1. Magnetic-Tape Controller (Nine-Track) Specifications (continued)

Power Requirements	+5V dc, 3A nominal
Operational Environment	+10 to +45 degrees C, 10 to 90 percent relative humidity without condensation

Table 1-2. Tape Transport Specifications

Height	24.5 inches
Depth	11.7 inches from mounting surface, 15.0 inches total
Width	19.00 inches
Weight	85 pounds
Mounting	Standard RETMA rack mounting
Tape Speed:	
Read/Write	25 inches per second
Rewind	75 inches per second
Tape Speed Variation:	
Instantaneous	±3 percent
Long-Term	±1 percent
Starting Time	17.25 ±0.75 milliseconds
Stopping Time	17.25 ±0.75 milliseconds
Input Power	115/230V ac, 200W, 48 to 400 Hz

(continued)

Table 1-2. Tape Transport Specifications (continued)

Operational Environment	+1.5 to +50 degrees C, sea level to 20,000 feet altitude, 15 to 95 percent relative humidity without condensation
Tape Width	1/2 inch
Tape Reel Size	10.5 inch diameter
Tape Type	1.5 mm base
Tape Tension	Eight ounces
Recording Density	800 bytes per linear inch of tape
Recording Format	9-channel, NRZ1 (nonreturn to zero, change on ones), IBM 2400-compatible

1.4 FUNCTIONAL DESCRIPTION

The MTC permits two basic operations: reading from and writing onto the tape. When the MTC is under program control, the computer initiates and the I/O instructions execute all data transfers. When operating with a BIC, the MTC can initiate data transfers by sending control signals to the BIC. The latter method is free of intervention by the computer program.

During reading, data are read from the tape in eight-plus-parity-bit bytes. The MTC checks the parity of each byte and arranges each pair of bytes into a data word. These words are transferred to the computer under BIC or program control. When using a BIC, the MTC communicates directly with the computer memory by cycle stealing.

During writing, data words are transferred to the MTC under BIC or program control. The MTC splits each word into two 8-bit bytes, generates odd parity bits for each byte, and transfers the bytes to the tape.

1.4.1 Tape Format

The format of the data on the tape conforms to the IBM 2400 nine-track NRZ1 (nonreturn to zero, change on ones) format. Each byte, consisting of eight data bits and one odd-parity bit, forms a column of bits across the tape. There are 800 bytes per linear inch of tape.

1.4.1.1 Tape Markers

Plastic markers on the uncoated side of the tape signal the beginning and end of the useful part of the tape. The markers are coated with adhesive on one side and aluminum on the other. The Beginning of Tape (BOT) marker is not more than 0.031 inch from and parallel to the bottom edge of the tape at least 10 feet from the beginning. The End of Tape (EOT) marker is not more than 0.031 inch from and parallel to the top edge of the tape at least 14 feet from the end. Figure 1-4 shows the correct placement of the markers for detection by the tape transport photocell.

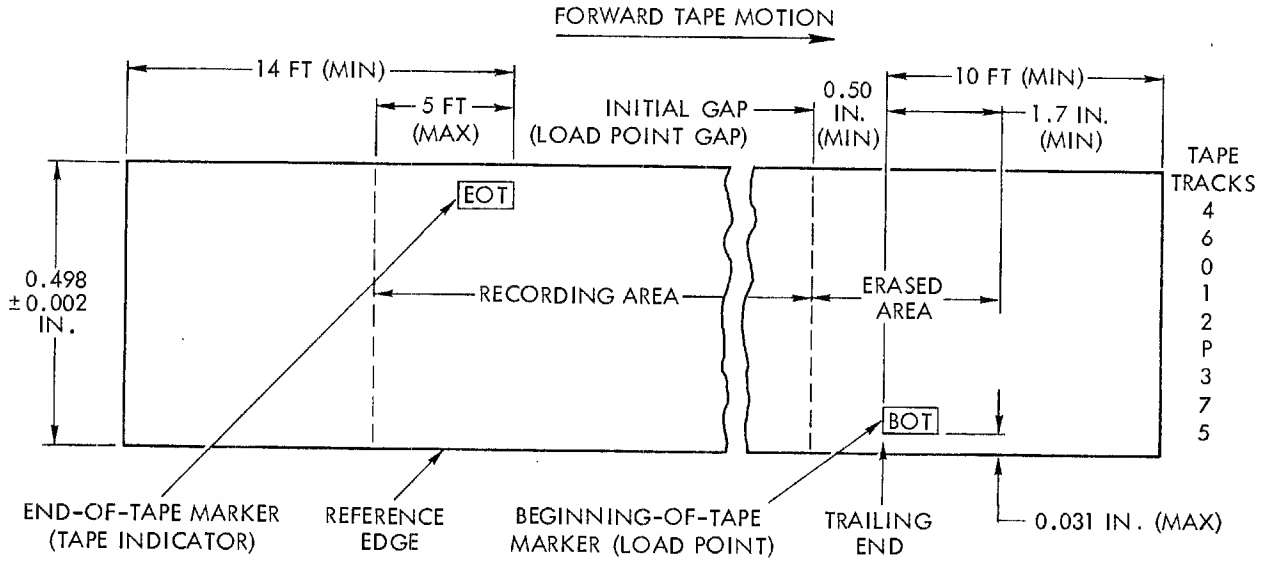


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FIGURE 1-4. Beginning and End of Tape Areas.

1.4.1.2 File Protection Device

To prevent accidental destruction of recorded data, a plastic ring must be in the groove in the tape reel when writing on the tape. The WRITE ENABLE indicator on the tape transport lights when the ring is in place and the tape under proper tension. If the ring is not in place, writing is disabled.

1.4.1.3 Tape Records

The data on the tape are divided into records. Each record can contain any number of bytes, but 18 data bytes is the minimum for IBM 2400-compatible records.

The data bytes are followed by three blank characters, a cyclic redundancy check (CRC) character, three more blank characters, and a longitudinal redundancy check (LRC) character as shown in figure 1-5.

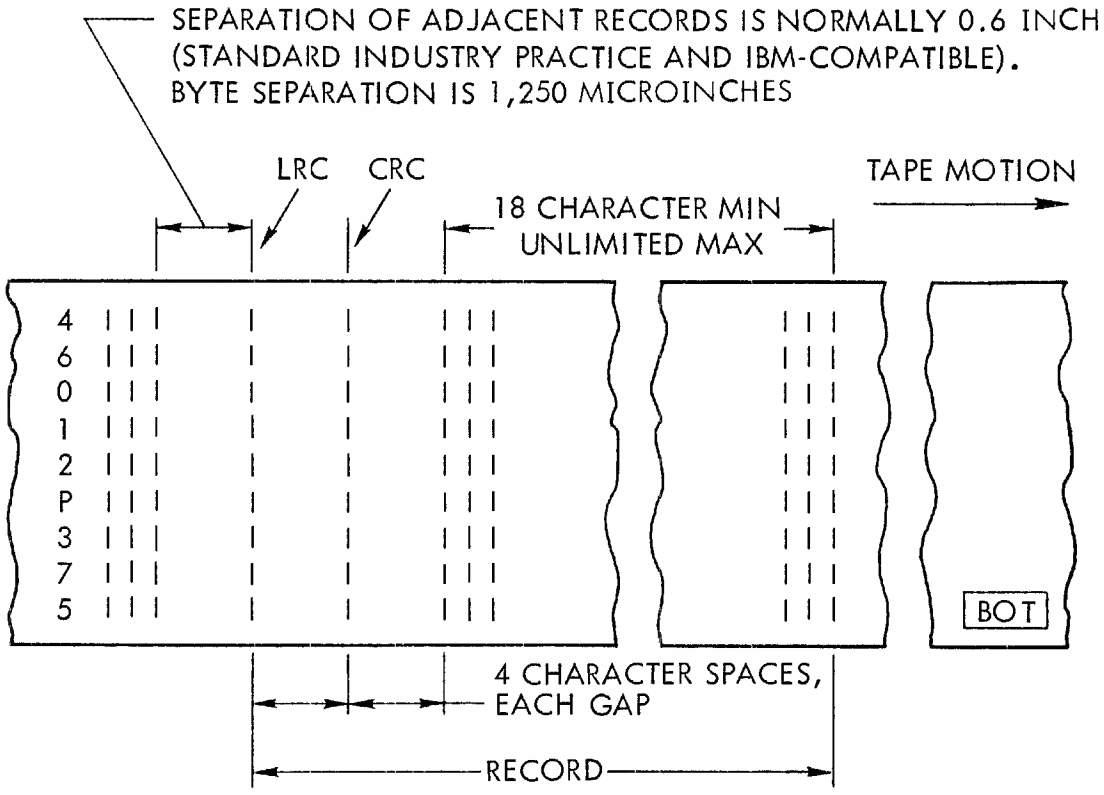

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FIGURE 1-5. Tape Record.

The CRC character is generated from the data bytes. It aids in detecting single-track errors and ensures that the LRC character is not zero. During reading, the CRC character is regenerated and compared with the written CRC character.

The LRC character is generated by adjusting the parity of each track to even parity for the record, including data bytes and the CRC character. Since the data bytes each have an odd-parity bit, the LRC also includes a vertical redundancy check (VRC). During reading, the LRC character is regenerated and compared with the written LRC character.

Data bytes are 1250 microinches apart. To be IBM-compatible, records are separated by 0.6 inch of blank tape.

The action taken upon detection of an error is under program control (see section 2).

1.4.1.4 Files and File Marks

A file is a group of one or more tape records. Files are separated by a file-mark record consisting of a file-mark character followed by seven blanks (absences of flux transition) and an LRC character.

1.4.2 Tape Controller Operation

As shown in figure 1-6, the MTC contains circuitry for:

a. Instruction decoding

b. Instruction storage

c. Sensing functions and response gating

d. Read-motion control

e. Read/write data control and write-motion control

f. Read/write data storage and error checking

g. Clock generation

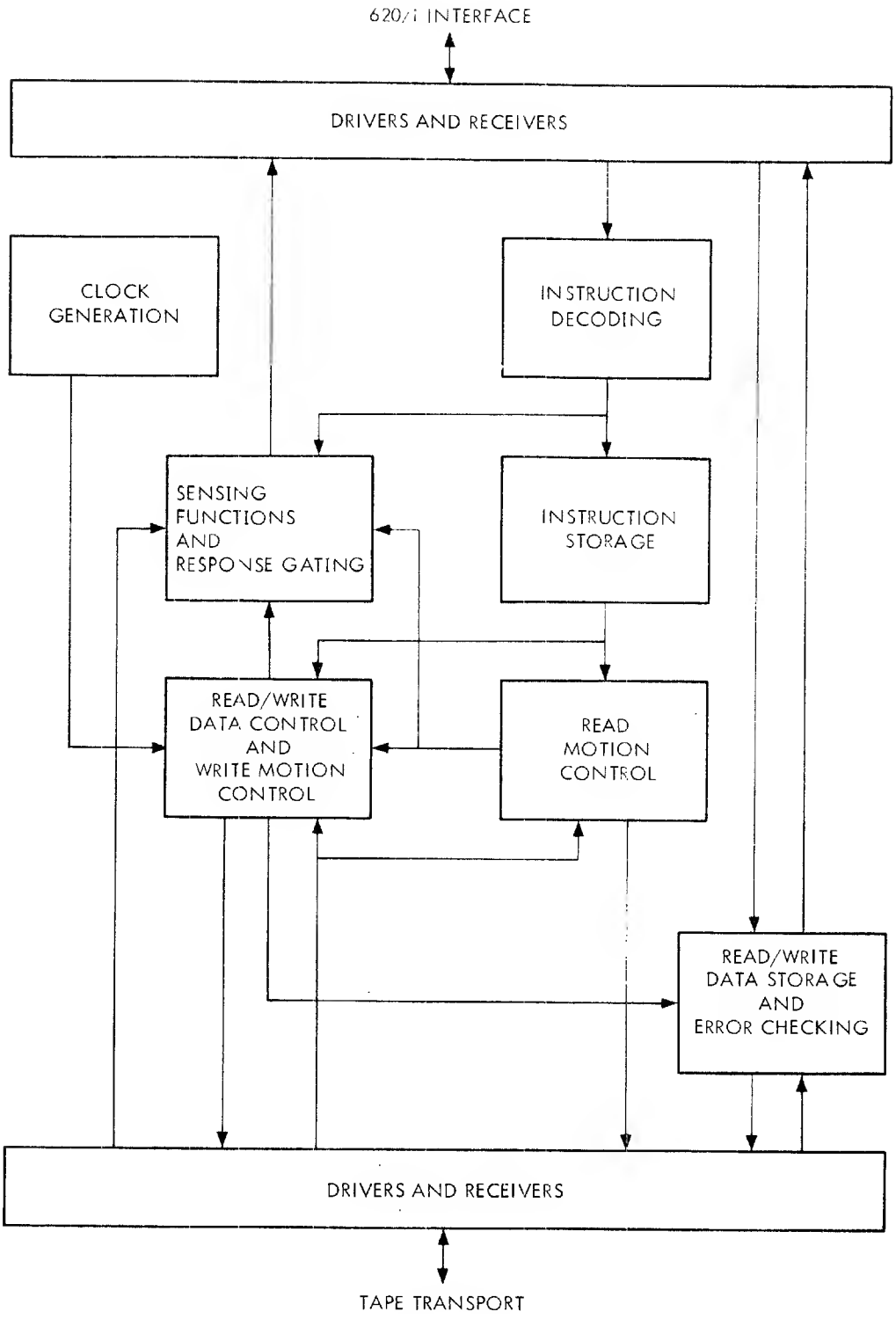

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FIGURE 1-6. Tape Controller, Functional Block Diagram.

1.4.2.1 Drivers and Receivers

The drivers and receivers form the interfaces between the MTC and the computer, and between the MTC and tape transports. They provide additional drive and one level of signal conversion.

1.4.2.2 Instruction Decoding and Storage

This logic decodes instructions from the receivers. If the instruction is a sense command, the decoding logic activates the sensing logic for transmission of the sense status to the computer. If the instruction is a motion command, it is stored in the instruction storage register.

1.4.2.3 Sensing Functions and Response Gating

This logic samples the status information and transmits it to the drivers under control of the instruction decoding register. Such status information indicates if the tape transport is ready, if the data storage registers are ready to receive, if a file mark is detected, or if the beginning or end of the tape is detected.

1.4.2.4 Read-Motion Control

The output of this logic initiates forward tape motion upon receipt of a Read One Record or Forward One Record instruction.

1.4.2.5 Read/Write Data Control and Write-Motion Control

The output of the write-motion control logic initiates forward tape motion upon receipt of a command to write. This logic also senses when the tape is up to speed and ready to transmit or receive data.

The read/write control logic monitors the data storage registers. It assembles bytes into words during reading operations or splits the words into bytes during writing operations. The logic also signals the sensing logic that the buffer is ready when the A register is full during reading operations or empty during writing operations.

1.4.2.6 Read/Write Data Storage and Error Checking

During writing, the data word is loaded into the A register, split into two 8-bit bytes, and transferred to the B register. Thus, two 16-bit words can be stored simultaneously in the data registers. One byte at a time is loaded from the B into the CB register and a parity bit is generated. The nine-bit byte is then transmitted through the drivers and written onto the tape.

During reading, the sequence is reversed. The data from the tape is sent through the receivers to the CB register, assembled two bytes at a time in the B register, and transferred to the A register. When the A register is full, the control logic (section 1.4.2.5) signals the sensing logic that the buffer is ready to transmit on the E bus.

Figure 1-7 shows the data storage registers.

The error-checking logic generates and checks parity bits (VRC), and LRC and CRC characters. As the data are read, odd parity is generated for each byte. When the last data byte of a record is received, the LRC and CRC characters are read from the tape and compared with the generated characters (figure 1-8).

1.4.2.7 Clock Generation

A crystal oscillator and synchronous countdown logic generate tape-system clock signals for driving the MTC.

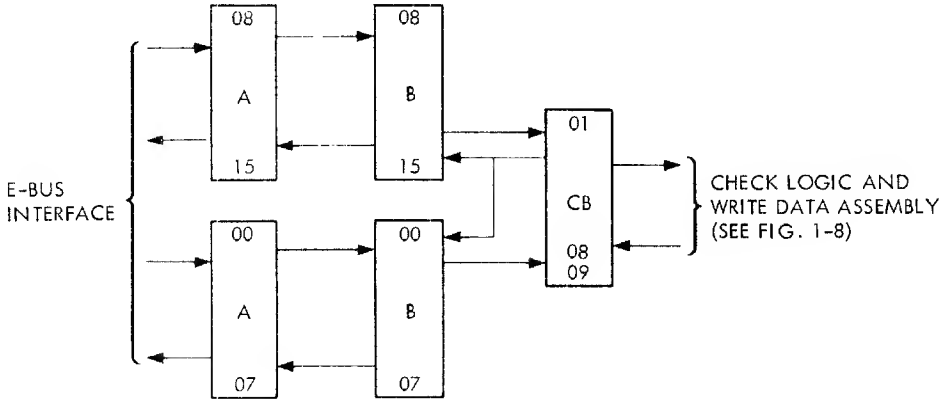

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FIGURE 1-7. Tape Controller Data Storage Registers.

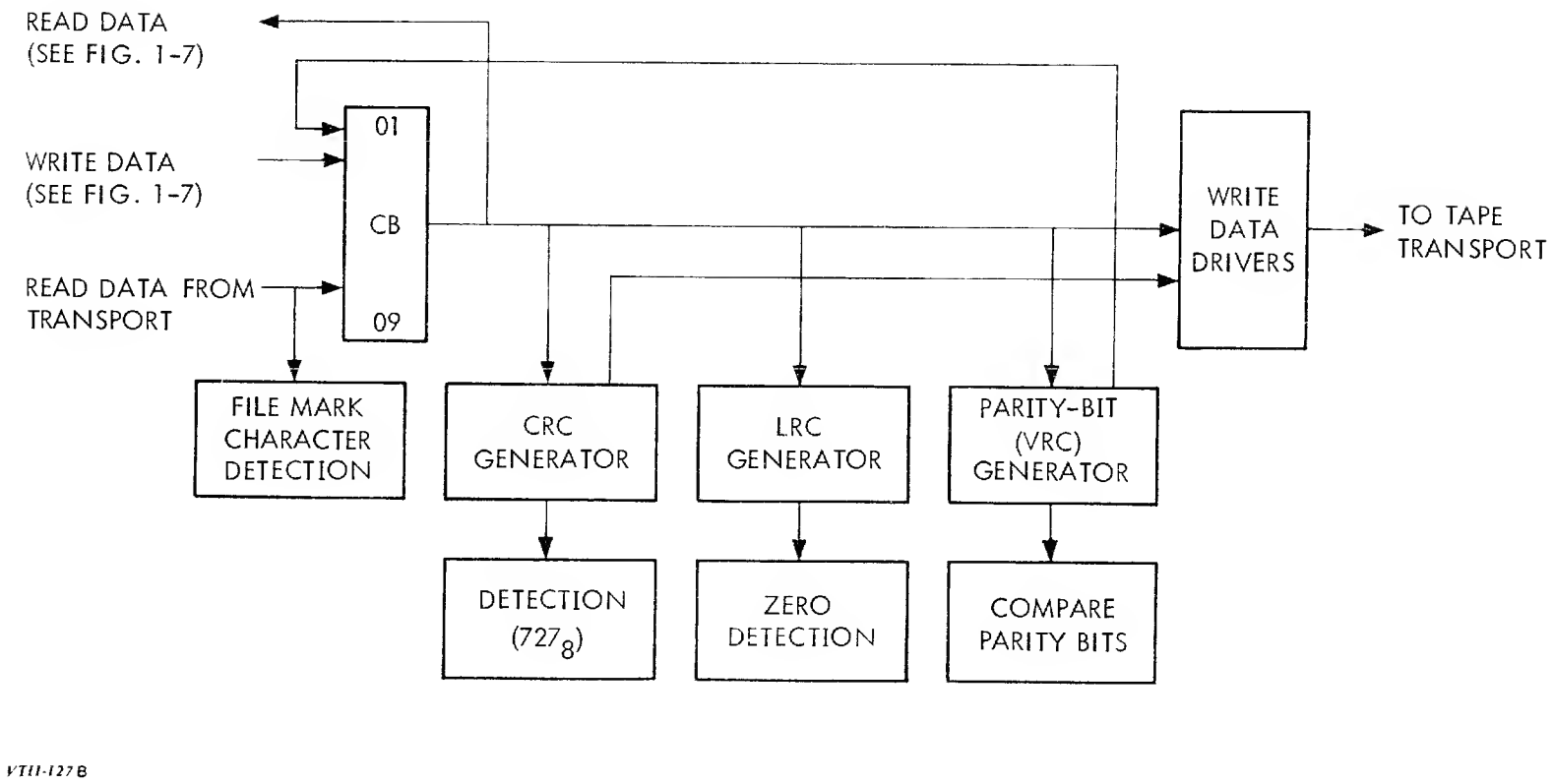


FIGURE 1-8. Check-Character Generation.

SECTION 2
PROGRAMMING

2.1 GENERAL

Characteristics of the magnetic-tape system that affect the programming of that system are:

a. That the A and B registers together have a capacity of two data words.

b. That the average data-transfer rate is 10,000 words (20,000 characters) per second.

c. That the computer requires at least 80 microseconds response time for either reading or writing.

d. The timing given in figure 2-1.

Figure 2-2 shows the format of a data word. High-order byte A is written onto or read from the tape before low-order byte B.

If SENSE switch 1 on the computer is off, tape records will be continuously read or written under program control. If SENSE switch 1 is on and SENSE switch 2 is off, the sequence is write/backspace or read/backspace. If SENSE switches 1 and 2 are both on, the sequence is write/backspace/read.

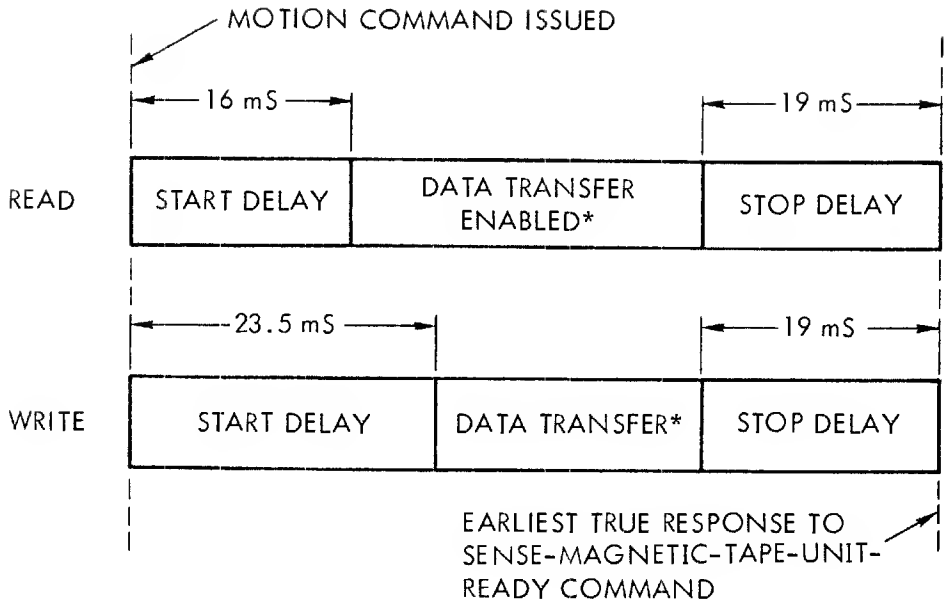
2.2 DESCRIPTIONS OF INSTRUCTIONS

Table 2-1 lists the MTC I/O instructions.

2.2.1 Read One Record (EXC 010)

This instruction starts the tape, reads characters serially into the MTC registers, and assembles them into two-byte words. It then signals the sensing logic when the buffer is ready to transmit the data to the computer.

Reading continues until either the specified number of characters has been read or the end of the record is reached. In either case, the entire record is checked for errors. The record can be a data record or a file mark.



*AVERAGE DATA TRANSFER RATE IS 10,000 WORDS (20,000 CHARACTERS) PER SECOND

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FIGURE 2-1. Programming Timing.

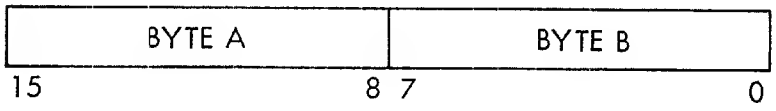

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FIGURE 2-2. Data Word Format.

Table 2-1. I/O Instructions for the Magnetic-Tape Controller

Mnemonic	Octal	Description
EXTERNAL CONTROL		
EXC 010	100010	Read One Record
EXC 0210	100210	Write One Record
EXC 0410	100410	Write File Mark
EXC 0510	100510	Forward One Record
EXC 0610	100610	Backspace One Record
EXC 0710	100710	Rewind
TRANSFER		
OME 010	103010	Output Memory to Magnetic Tape Buffer
OAR 0110	103110	Output A Reg to Magnetic Tape Buffer
OBR 0210	103210	Output B Reg to Magnetic Tape Buffer
IME 010	102010	Input Magnetic Tape Buffer to Memory
INA 0110	102110	Input Magnetic Tape Buffer to A Register
INB 0210	102210	Input Magnetic Tape Buffer to B Register
CIA 0510	102510	Input Magnetic Tape Buffer to A Register Cleared
CIB 0610	102610	Input Magnetic Tape Buffer to B Register Cleared
SENSE		
SEN 010	101010	Sense Tape Error
SEN 0110	101110	Sense Buffer Ready
SEN 0210	101210	Sense Tape Unit Ready
SEN 0310	101310	Sense File Mark
SEN 0410	101410	Sense Odd-Length Record
SEN 0510	101510	Sense End of Tape
SEN 0615	101610	Sense Beginning of Tape
SEN 0710	101710	Sense Rewinding
TRANSPORT SELECTION		
EXCB 0110	104110	Select Tape Transport 1
EXCB 0210	104210	Select Tape Transport 2
EXCB 0310	104310	Select Tape Transport 3
EXCB 0410	104410	Select Tape Transport 4

2.2.2 Write One Record (EXC 0210)

This instruction starts the tape; signals the computer when the MTC can receive data; transfers the data to the MTC with an output instruction; or, using the BIC, separates each word into two bytes, generates an odd-parity bit for each byte, and writes the data onto the tape. This continues until no more data are received by the MTC at the normal transfer rate, at which time the check characters are generated and written onto the tape and the tape stopped.

2.2.3 Write File Mark (EXC 0410)

This instruction writes a file-mark record, including gaps and check characters. There is no data transfer between the MTC and the computer.

2.2.4 Forward One Record (EXC 0510)

This instruction advances the tape one record. It does not require any computer time or transfer data. However, the record skipped is checked for errors.

2.2.5 Backspace One Record (EXC 0610)

This instruction backspaces the tape one record. It does not require any computer time, transfer data, or check for errors.

2.2.6 Rewind (EXC 0710)

This instruction rewinds the tape to the BOT marker and stops it.

2.2.7 Sense Tape Error (SEN 010)

This instruction should be issued only when the tape unit is stopped and no motion instruction has been issued, i.e. when the Tape Unit Ready signal is true (section 2.2.9). The Sense Tape Error instruction senses the error signal generated by:

a. A parity (VRC, LRC, or CRC) error detected during execution of a Read One Record or Forward One Record instruction.

b. A Write One Record or Write File Mark instruction issued when the file-protection ring is not in place on the tape reel.

c. The tape transport leaving the ready state during the execution of any instruction.

2.2.8 Sense Buffer Ready (SEN 0110)

During reading, a true response to this instruction indicates that the MTC is ready to transmit a word. During writing, a true response indicates that the MTC is ready to receive a word. This instruction is not used with the BIC.

2.2.9 Sense Tape Unit Ready (SEN 0210)

A true response to this instruction indicates that the tape is stopped and the tape transport is ready to receive external control instructions.

2.2.10 Sense File Mark (SEN 0310)

A true response to this instruction indicates that the record checked by the last Read One Record or Forward One Record instruction was a File Mark instruction. The first motion instruction issued after detection of a file mark resets the FILE MARK indicator.

2.2.11 Sense Odd-Length Record (SEN 0410)

A true response to this instruction indicates that the last character of a record having an odd number of data bytes has been read. The lower-order byte of the last word is ignored. The first motion instruction issued after detection of an odd-length record resets the ODD LENGTH indicator.

2.2.12 Sense End of Tape (SEN 0510)

A true response to this instruction indicates that the EOT marker has been detected. The EOT detector is reset by this instruction, or by the Backspace One Record or Rewind instructions.

2.2.13 Sense Beginning of Tape (SEN 0610)

A true response to this instruction indicates that the tape is stopped at the BOT marker.

2.2.14 Sense Rewinding (SEN 0710)

A true response to this instruction indicates that the tape transport is rewinding the tape. Upon completion of the rewinding, the REWIND indicator is reset and the BOT indicator is set (section 2.2.13).

2.2.15 Select Tape Transport 1 (or 2, 3, or 4) (EXCB Instructions)

This instruction selects one of up to four tape transports for connection to the MTC if the transport is in on-line status. System reset automatically connects transport 1 to the MTC.

2.3 SAMPLE PROGRAM

Figure 2-3 is a program for writing a block of characters onto the tape and reading them back. The size of the block can vary.

The initial conditions for execution of the program are that the A register must contain the block length and the B register must contain data.

Figure 2-4 is a flow chart for writing onto the tape, and figure 2-5 is a flow chart for reading from the tape.

```
00000    050057    ,STA     SIZE      SIZE OF BLOCK
00001    101210    ,SEN     ,0210     SENSE TAPE TRANSPORT READY
00002    000005R
00003    001000    ,JMP
00004    000001R
00005    100210    ,EXC     ,0210     WRITE ONE RECORD BINARY
00006    010057    ,LDA               SIZE OF BLOCK
00007    101110    ,SEN     ,0110     SENSE BUFFER READY
00010    000013R
00011    001000    ,JMP
00012    000007R
00013    103210    ,OBR     ,0010     DATA
00014    005311    ,DAR               DECREMENT BLOCK SIZE
00015    001010    ,JAZ               A REGISTER ZERO
00016    000021R
00017    001000    ,JMP
00020    000007R
00021    001100    ,JSS1              SENSE SWITCH 1
00022    000025R
00023    001000    ,JMP
00024    000001R
00025    101215    ,SEN     ,0210     SENSE TAPE TRANSPORT READY
00026    000031R
00027    001000    ,JMP
00030    000025R
00031    100610    ,EXC     ,0610     BACKSPACE ONE RECORD
00032    001200    ,JSS2              SENSE SWITCH 2
00033    000036R
00034    001000    ,JMP
00035    000001R
00036    101210    ,SEN     ,0210     SENSE TAPE TRANSPORT READY
00037    000042R
00040    001000    ,JMP
00041    000036R
00042    100010    ,EXC     ,0010     READ ONE RECORD BINARY
00043    010057    ,LDA     SIZE      BLOCK LENGTH
00044    101110    ,SEN     ,0110     SENSE BUFFER READY
00045    000050R
00046    001000    ,JMP
00047    000044R
00050    102010    ,IME               READ BUFFER INTO MEMORY
00051    000060R
00052    005311    ,DAR               DECREMENT BLOCK SIZE
00053    001010    ,JAZ               A REGISTER ZERO
00054    000001R
00055    001000    ,JMP
00056    000044R
00057                                  BLOCK LENGTH
00060                                  DATA
```

FIGURE 2-3. Sample Tape System Program.

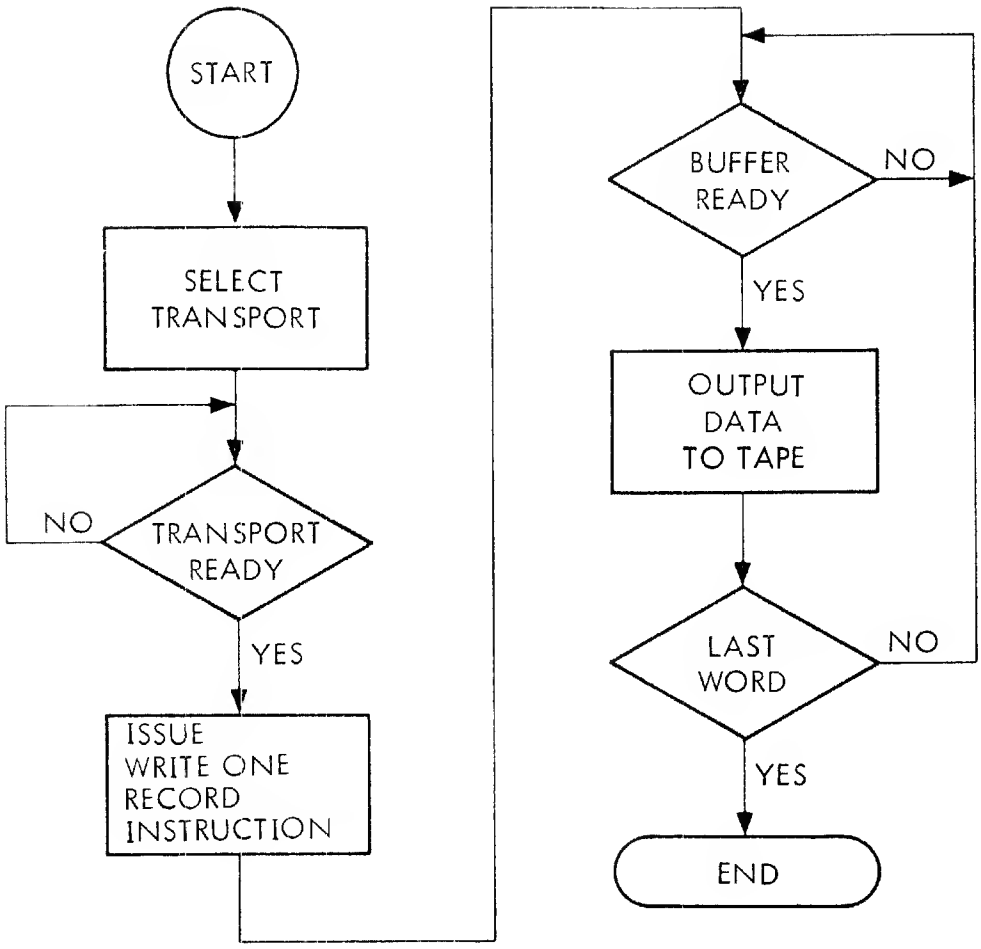

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FIGURE 2-4. Flow Chart for Writing onto the Tape.

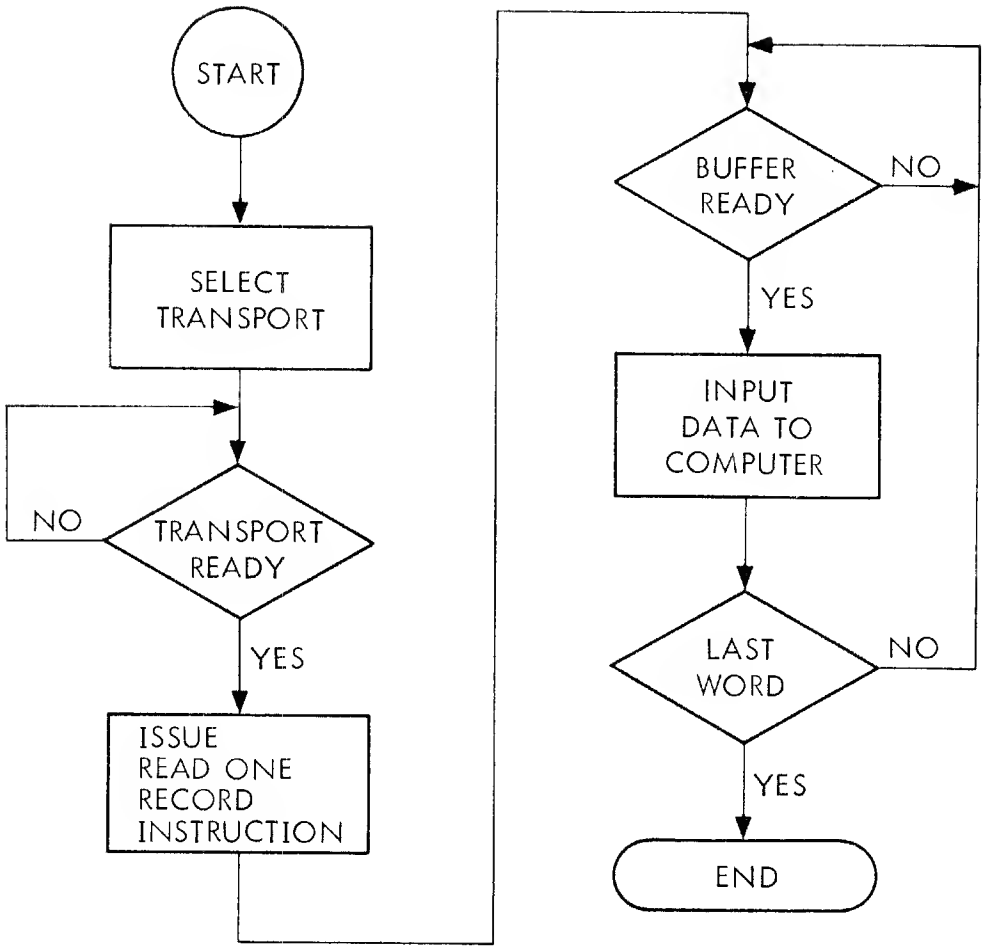

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FIGURE 2-5. Flow Chart for Reading from the Tape.

SECTION 3
INSTALLATION

3.1 GENERAL

The magnetic-tape system is installed by Sperry Univac customer service engineers. The appendix of this manual contains timing and mnemonic information.

3.2 PREINSTALLATION REQUIREMENTS

Mount the tape transports in standard 19 inch racks placed so that they can be connected to the MTC by the tape-transport cable. This cable has a maximum length of 20 feet. If the system has more than one tape transport, the total length of all tape-transport cables cannot exceed 20 feet.

3.3 INSTALLATION

Install the MTC boards in adjacent slots of the expansion chassis. Insert them into the mounting guides with the component sides of the boards on your left as you face the rear of the chassis.

Apply moderate pressure to the boards, forcing the 122-terminal edge connectors to seat firmly in the mating connectors on the chassis backplane. Take care to apply equal pressure to the upper and lower halves of the boards to prevent damage to the backplane connectors or to the nylon guides.

To remove the boards, use a board puller (Tichener 1731 or equivalent).

The MTC end of the tape transport cable has two connectors. Connect the one labeled P1 to connector J1 of MTC board 1 (part number 44P0232), and the one labeled P2 to connector J2 of MTC board 2 (part number 44P0233).

Connect the other end of the tape-transport cable to the tape transport if there is only one transport, or to the party-line cable adapter if there are more than one tape transport. Two transports require one adapter, three transports require two adapters, and four transports require three adapters, connected in series. Figure 3-1 shows the cabling for a system with two tape transports.

The I/O cable has its termination shoe in the chassis at J32. If no BIC is installed, or if the BIC is in the same chassis as the MTC, the I/O cable comes directly from the 620/i. In these cases, termination shoe J36 is not used (figure 1-2).

If a BIC is installed in a chassis other than that containing the MTC, the I/O cable comes from that chassis and is connected to J32 of the one containing the MTC. In this case, the B cable of the BIC connects J1 on the BIC with J36 on the chassis containing the MTC (figure 3-2).

For further installation information, refer to engineering document 01A0869.

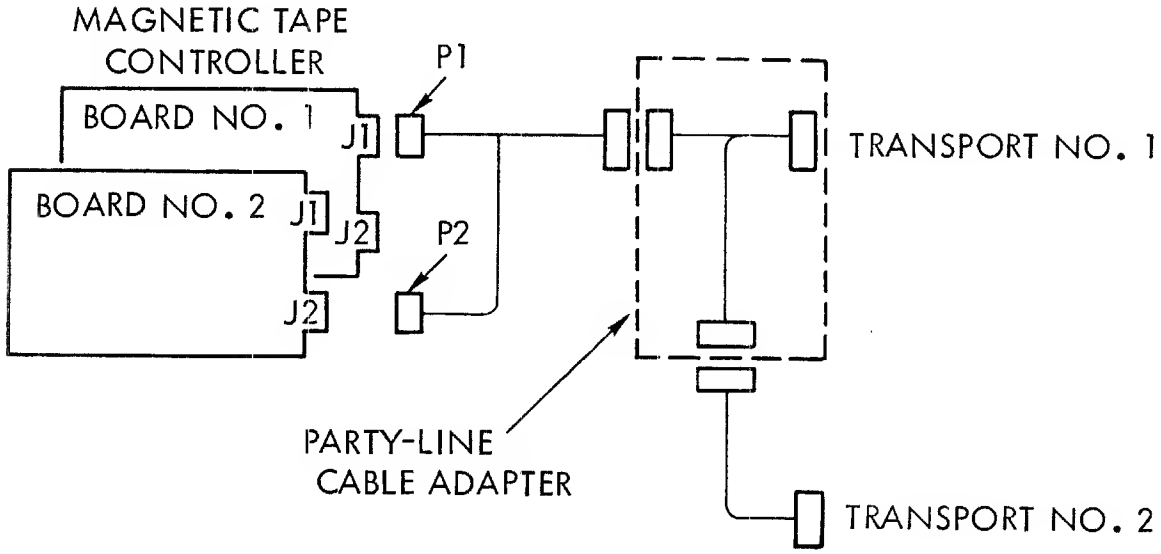

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FIGURE 3-1. Party-Line Cabling with Two Transports.

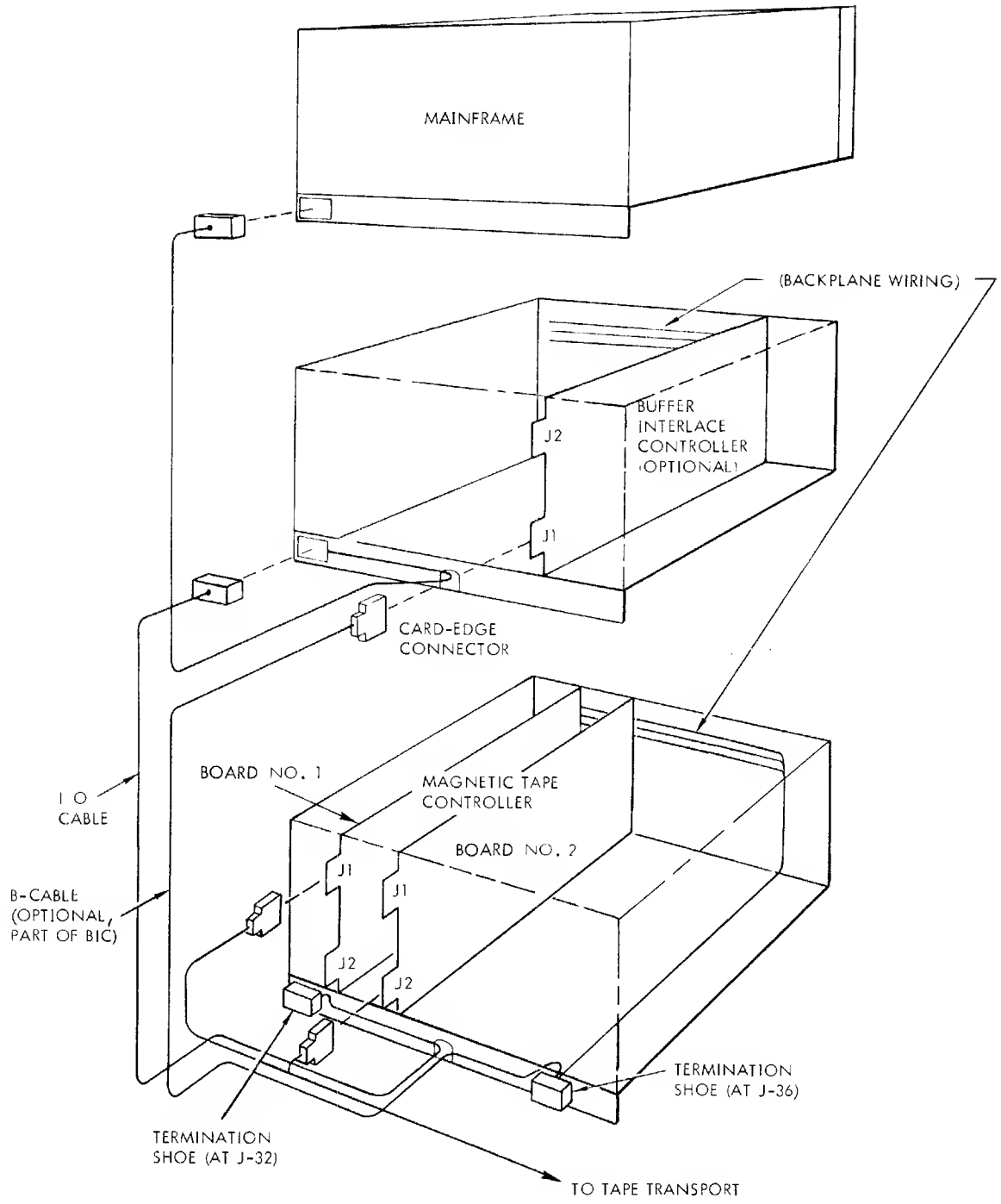


FIGURE 3-2. Cabling with BIC and MTC in Different Chassis.

SECTION 4
MAINTENANCE

4.1 GENERAL

This section tells how to adjust the time-delay potentiometers on the MTC and how to perform diagnostic maintenance.

4.2 POTENTIOMETER ADJUSTMENT

Card 1 of the MTC holds nine adjustable time-delay potentiometers, R1-R9, as indicated on the assembly drawing 44D0232 in the System Maintenance Manual. Adjust these potentiometers to the delay times shown in table 4-1, using the test points shown.

In troubleshooting, these adjustments are made after running the diagnostic program, as explained in the next paragraph.

4.3 TROUBLESHOOTING

MTC troubleshooting procedures make use of the programs in the document "Magnetic Tape Diagnostic - Version 02.0." These programs are:

a. Magnetic-tape GROW program

b. Magnetic-tape high-density program

c. Forward/backspace one record program

d. Write/sense file-mark program

Each of the following tests constitutes one item in the complete series of diagnostic routines on the MTC. Performing this sequence of tests is the usual method of troubleshooting the MTC:

a. Perform the diagnostic programs according to the instructions provided with them in Version 02.0.

b. Adjust the potentiometers according to section 4.2 to obtain the best oscilloscope resolution possible for the output pulses of the one-shots.

c. Execute the program given in figure 4-1, or its equivalent.

d. Manually execute instructions EXC 0210 and 0410, observing the TDER flip-flop on the scope, the tape on the transport, and the computer's response to the Sense Tape Error (SEN 010) instruction.

e. Simulate errors by grounding key points in the check-character-generation logic during a normal read/write data control operation.

f. Simulate a transport not ready. This is done by grounding RDY+ during any motion instruction except rewind. This sets flip-flop TMER.

g. Execute each EXCB instruction manually, observing the output at each of the four line drivers as each instruction is executed. A pullup resistor on each driver output is required so that the level change can be observed on the oscilloscope.

h. Execute a Write One Record (EXC 0210) instruction. Ignore the BUFFER READY indicator and wait for a true response to the Sense Tape Unit Ready (SEN 0210) instruction. When the unit is ready, execute the Sense Odd-Length Record (SEN 0410) instruction. The response should be true. The next motion instruction should reset the indicator.

Table 4-1. Time Delay Adjustment

Potentiometer	Test Point Location	Delay Time (Milliseconds)
R1	G10-8	150
R2	H10-8	0.5
R3	K10-8	16
R4	L10-8	250
R5	M10-8	19
R6	N10-8	0.425
R7	R10-8	0.175
R8	S9-8	60
R9	T9-8	23.5

Memory Location	Octal Code	Comments
500	100021	Init. BIC
501	103020	Load BIC I Reg.
502	541	
503	103021	Load BIC F Reg.
504	542	
505	101210	SEN MTU Rdy
506	511	
507	1000	Jump
510	505	
511	100020	BIC Activate Enable
512	100210 (100010)	WOR (ROR)
513	101020	SEN BIC Not Busy
514	517	
515	1000	Jump
516	513	
517	101021	SEN Abnormal Stop
520	540	
521	1100	JSS1
522	525	
523	1000	Jump
524	500	
525	0000	HALT
526	XXXXX	Write Data (Read Data)
527	⋮	
530	⋮	
531	⋮	
532	⋮	
533	⋮	
534	⋮	
535	⋮	
536	⋮	
537	XXXXX	
540	0000	HALT (Abnormal Stop)
541	526	Initial Address
542	537	Final Address
543		
544		
546		
547		

FIGURE 4-1. BIC Test Program for the MTC.

APPENDIX

MNEMONICS DEFINITION LIST AND TIMING DIAGRAMS

The following is a list of mnemonics with definitions and logic-diagram locations. The location designations consist of a logic-diagram sheet number and zone on that sheet.

MNEMONIC DEFINITION LIST

Mnemonic	Definition	91C0032	91C0033
ADDX-	Device address (EB00-EB05 and IUAX-)		16C2
ARCm	A register control flip-flops (m = 1, 2)	3B1	
ARCOn	A register control flip-flops decoded (n = 0,...3)	3D4	
ARn	Flip-flop n of A register (n = 00, 01,...15)		17-18
BCn	Flip-flop n of bit counter (n = 1, 2, 3)		13D
BCCLK	Bit counter clock		13C4
BCDX-B	BIC interface signal -- deactivate buffer controller	6C2	
BOR	Backspace one record	10D1	
BRn	Flip-flop n of B register (n = 00, 01,...15)		19-20
BRCm	B register control flip-flops (m = 1, 2)	4D1-2	
BRCOn	B register control flip-flops decoded (n = 0,...3)	4B3,4	
CBn	Flip-flop n of character buffer register (n = 1, 2,...9)		9-10
CBCNT	Character buffer character counter	4C1	

Mnemonic	Definition	91C0032	91C0033
CDCX-B	BIC interface signal -- controlled device connected	6D1	
CGCLK	CRC character generator clock		9A3
CKEOTD	Clock end-of-tape detection flip-flop	12B4	
CLKSLT	Clock transport selection register	A83	
CLKWRA		10B2	
CLKWRB	Clock write/read status flip-flop	10A2	
CLKWRS		10B2	
CRCER	CRC error indicator		9B3
CRCGn	CRC character generator flip-flop n		7-9
CRCRES	CRC character generator reset		7C4
CRCS	Select CRC charactpr for output to transport write data lines		3D1
CSDTX	Clock input to synchronize data transfer out	6D3	
DCEX-B	BIC interface signal -- connect device	6B4	
DESX-B	BIC interface signal -- stop device	6A4	
DLn	Flip-flop n of data logic control flip-flops (n = 1,...4)		3C1-2
DLDn	Data logic flip-flops decoded (n = 00,...17)		4X3
DRBC	Direct reset of the BC flip-flop		13C4

Mnemonic	Definition	91C0032	91C0033
DRRSC	Direct reset of the RSC flip-flop		12B2
DRTC1	Direct reset of the TC1 flip-flop		
DRWC	Direct reset of the WC flip-flop		14C4
DRYX-I	Data ready signal (computer)	6C4	
DSARn	Direct set of flip-flop ARn (n = 00, 01...15)		17-18
DSBRn	Direct set of flip-flop BRn (n = 00, 01,...15)		17-18
DSCBn	Direct set of flip-flop CBn (n = 1,...9)		9-10
DSEL	Select data (CB register) for output to write data lines of transport		
DSTDER	Direct set of the TDER flip-flop		20B2
DSTMER	Direct set of the TMER flip-flop	12D3	
DTCLK	Clock for DTIX and DTOX flip-flops	5A1	
DTI	Data-transfer-in (to computer)		16A2
DTIX	Data-transfer-in (to computer) flip-flop	5C1	
DTOX	Data-transfer-out (from computer) flip-flop	5B1	
EBn	E bus data/address signals (n = 06,...08, 11,...15)	5x4	
ENDm	End-of-record/end-of-file read control logic flip-flops (m = 1,...4)	1D2,3,4	
ENDn	END flip-flops decoded (n = 00, 02, 03, 05,...07, 11, 12)	2x3	

Mnemonic	Definition	91C0032	91C0033
END+	End of record or end of file detected on previous ROR, FOR, or BOR instruction		
EOR1+	End-of-record counter decoded -- bit time number 1		13B1
EOR5	End-of-record counter decoded -- bit time number 5		13B3
EOTD	End-of-tape detection flip-flop	12A3	
EOT-T	End-of-tape signal from transport	7C4	
ERDL	Enable read data logic (ROR + FOR)	10B3	
EWDL	Enable write data logic (WOR)	10C3	
FDGAP	Forward data gap	9B3	
FMCD	File mark character detection	1A3	
FOR	Forward one record	10D2	
FRYX-1	Function ready signal from computer	6C4	
FTAD	Turnaround delay flip-flop	14A3	
FUNCn	One of eight decodings of EB06, 07, 08 lines	11x3	
FUN67	FUNC6 + FUNC7	12A4	
FWD	Any forward-motion instruction (WOR + WFM + ROR + FOR)		
GCRC1	Generate CRC character	9B3	
GCRC2	Generate CRC character		9A3
GNDn	Signal ground n (n = 00,...46)		various
IUAX-I	Interrupt acknowledgement from computer		16B2

Mnemonic	Definition	91C0032	91C0033
Jxxxx+	J input to a 7473 flip-flop called xxxx	various	
Kxxxx+	K input to a 7473 flip-flop called xxxx	various	
LAB	Load A register into B register		20B4
LBA (H or L)	Load B register into A register (H = high, L = low)		18A3
LBHCB	Load BR08 through BR15 into CB register		20A3
LBLCB	Load BR00 through BR07 into CB register		20A3
LBRCB	Load CB9 from B register		10A2
LCBBH	Load CB register from BR08 through BR15		20C3
LCBBL	Load CR register from BR00 through BR07		20B3
LCRCG	Load CRC generator		5A3
LDP-T	Loadpoint (BOT) indicator signal from transport	7B4	
LEBA	Load E bus data into A register		18C3
LGCLK	LRCO character generator clock		5A4
LRCER	LRC error indicator		5A1
LRCGn	LRC character generator flip-flop n		5D
LRD	Load read data into CB register		12C4
MCLK	Master clock (2.78 MHz) generated from crystal oscillator		14A3

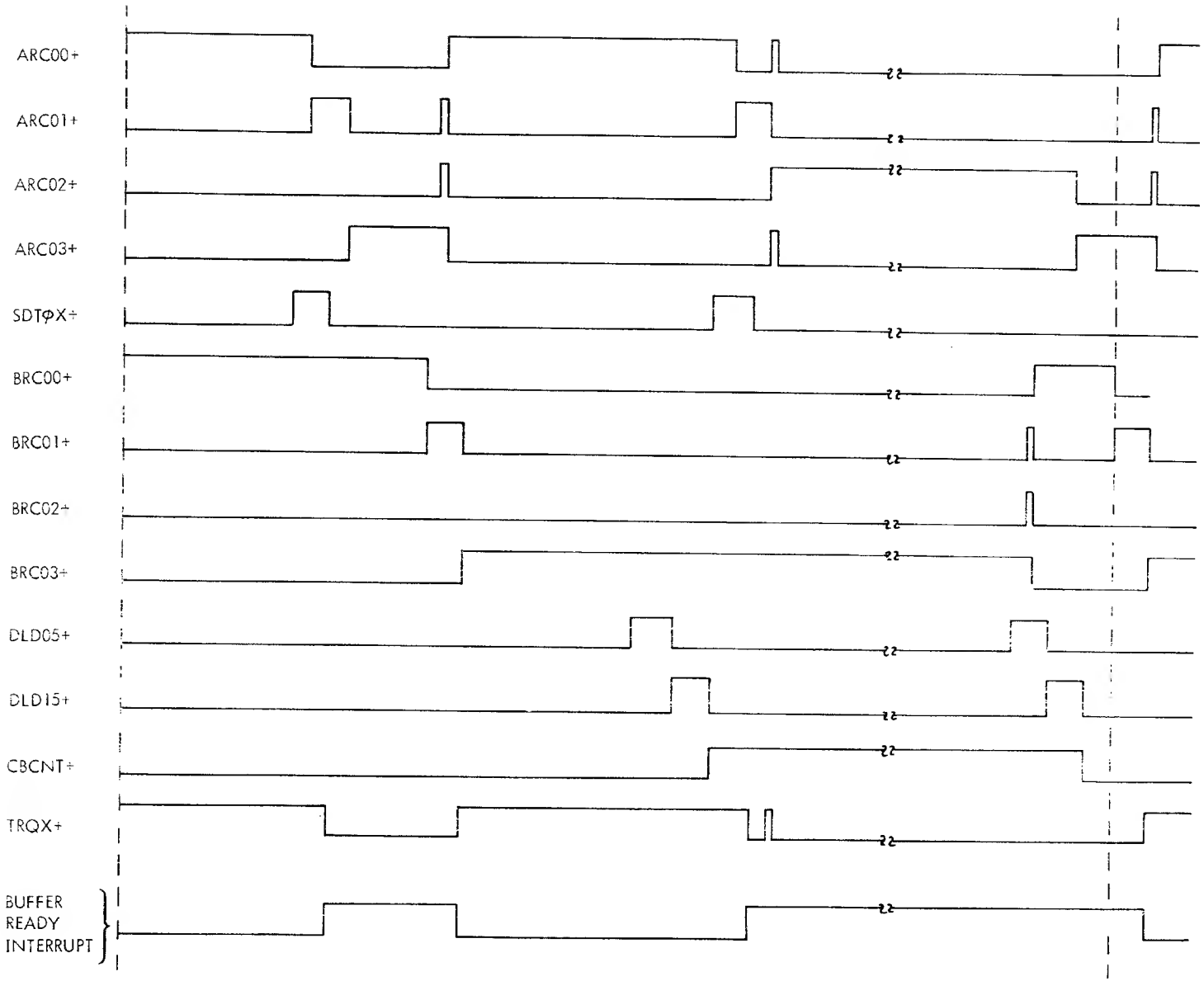
Mnemonic	Definition	91C0032	91C0033
MTCD1	MTC clock decoder No. 1 (about 10 usec before end of TC counter cycle)		12B3-4
MTCD2	MTC clock decoder No. 2 (terminates TC counter cycle)		11A1
OLR	Odd-length record indicator flip-flop	11C1	
RAR (H or L)	Reset A register (H = high, L = Low)		18B3
RBR (H or L)	Reset B register (H = high, L = low)	4B1	
RCB	Reset CB register		12D3
RDn	Read data line n from tape transport		1-2
RDACC	Read data accepted (by computer)	5A3	
RDD1	Read-data detection one-shot (reverse)	9D3	
RDD2	Read-data detection one-shot (forward)	9C3	
RDS-T	Read-data strobe from transport	7D4	
RDSTB	Read strobe from transport (generated from RDS-T)	7C3	
RDY-T	Transport READY TO ACCEPT COMMANDS indicator from transport	7C4	
RETn	Twisted-pair ground return		various
RHEADn	Supply voltage to discrete component mounting board n (n = 1, 2, 3)		various
RHEGNDn	Signal ground to discrete component mounting board n (n = 1, 2, 3)		various

Mnemonic	Definition	91C0032	91C0033
RLRCG	Reset LRC character generator		5B4
ROR	Read one record	10D4	
RSCn	Read strobe synchronization counter (n = 1, 2)		12C2
RSYNC	Resynchronize controller counters (resets counters to zero)		11B3
RWC-T	Rewind instruction to transport	8C3	
RWD-T	Rewinding indicator from transport	7B4	
RWND	Rewind instruction storage flip-flop	10D1	
SDEC	Clock for setting data error flip-flop (TDER)		20A2
SDTOX	Synchronize data transfer out	6D3	
SENS+	Output of sense response OR function (positive true)	11C2	
SERX-1	Sense command response to E bus	6B4	
SFC-T	Synchronous forward-motion instruction to transport	8D4	
SHCYC	Short cycle flip-flop used for resetting TC counter to zero at end of cycle		11B3
SLTn-T	Select lines to transport (n = 1,...4)	8x2	
SRC-T	Synchronous reverse instruction to transport	8C4	
SRDACC	RDACC signal synchronized with TCLK	5A2	
SRS	RDSTB signal synchronized with TCLK		12C2

Mnemonic	Definition	91C0032	91C0033
STLWD	Start long write/delay one-shot. Write file mark start delay or write first record after BOT marker	13B3	
STPDY	Stop delay one-shot	14C3	
STPM	Stop motion one-shot	14B2	
STRDM	Start read motion one-shot	13D3	
STRIM	Start read initial motion one-shot (first record after BOT marker)	13A3	
STRT	Start signal -- indicates that tape speed in increasing	13D1	
STSU	TSU signal synchronized with TCLK	14D4	
STWM	Start write motion	13A2	
SX	SYRT + XCX10	12C1	
SYRT-1	System reset from computer	6B3	
TAD	Turnaround delay one-shot	14A1	
TAKX-B	BIC interface signal -- data transfer request acknowledgement	5D2	
TCn	MTC clock flip-flop n (n = 001, 002, 004, 008, 016, 032, 064, 128)		11x1-2
TCCLK	Clock for MTC counter		11B3
TCLKx	MTC logic clock (x = A, B, C, D, E, F)		various
TCRES	Reset for MTC counter flip-flops		11B2
TCWC	MTC writing clock -- 0.72 usec clock pulse generated just after beginning the 20 kHz clock cycle		14C1

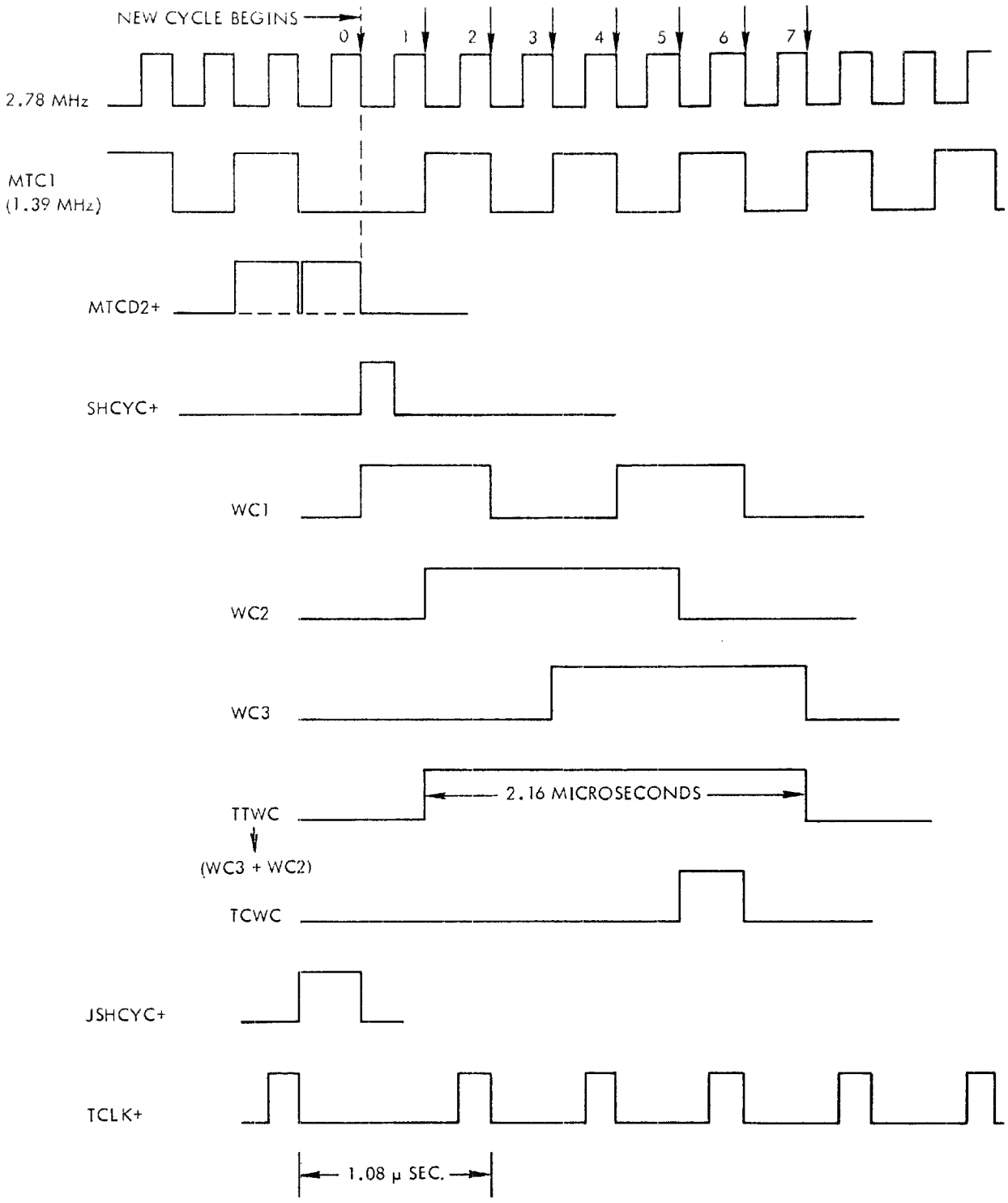
Mnemonic	Definition	91C0032	91C0033
TDER	Tape data error flip-flop		20A1
TMER	Tape motion error flip-flop	12C3	
TPUR	Tape unit ready for instructions	13C1	
TRQX-B	BIC interface signal data transfer request	6B1	
TS	TMER + SYRT	9C2	
TSR	TMER + SYRT + RSYNC	9C2	
TSS	TMER + SYRT + STPM	9C2	
TSSA	TMER + SYRT + STPM		
TSSR	TMER + SYRT + STPM + RSYNC	9A2	
TSU	Tape up to speed	13C1	
TSXn	TMER + SYRT + XCX10 (n = 1, 2, 3)	9Bx	
TTCn	Toggle TC flip-flop n (n = 001, 002, 004, 008, 016, 032, 064, 128, 256)		11C-D
TTWC	Tape transport writing clock. A 2.16 usec pulse generated just after beginning the 20 kHz clock cycle		14A1
TVCH	Tape velocity changing	13C1	
TWDn-T	Transport write-data line n (n = 1,...9)		2-3
VRC	Odd-parity bit generated from CB register outputs		6D1
VRCER	VRC error indicator		6C1
WARS-T	Write amplifier reset to transport. Generates LRC character at end of write operation	8A3	

Mnemonic	Definition	91C0032	91C0033
WC	WOR + WFM	10C3	
WCn	Write-clock flip-flop n (n = 1, 2, 3)		14D3-4
WDS-T	Write-data strobe to transport	8B3	
WDTO	Write-data transfer output enabler (enables write control signals)	8B4	3D2
WFM	Write file mark	10D3	
WIR	Write initial record (WOR . LDP)	13B4	
WOR	Write one record	10D3	
WRS-T	Write/read status to transport	8B4	
XCISI	External control instruction storage register idle	12B2	
XCX10	Any EXC command directed to tape controller	5C2	



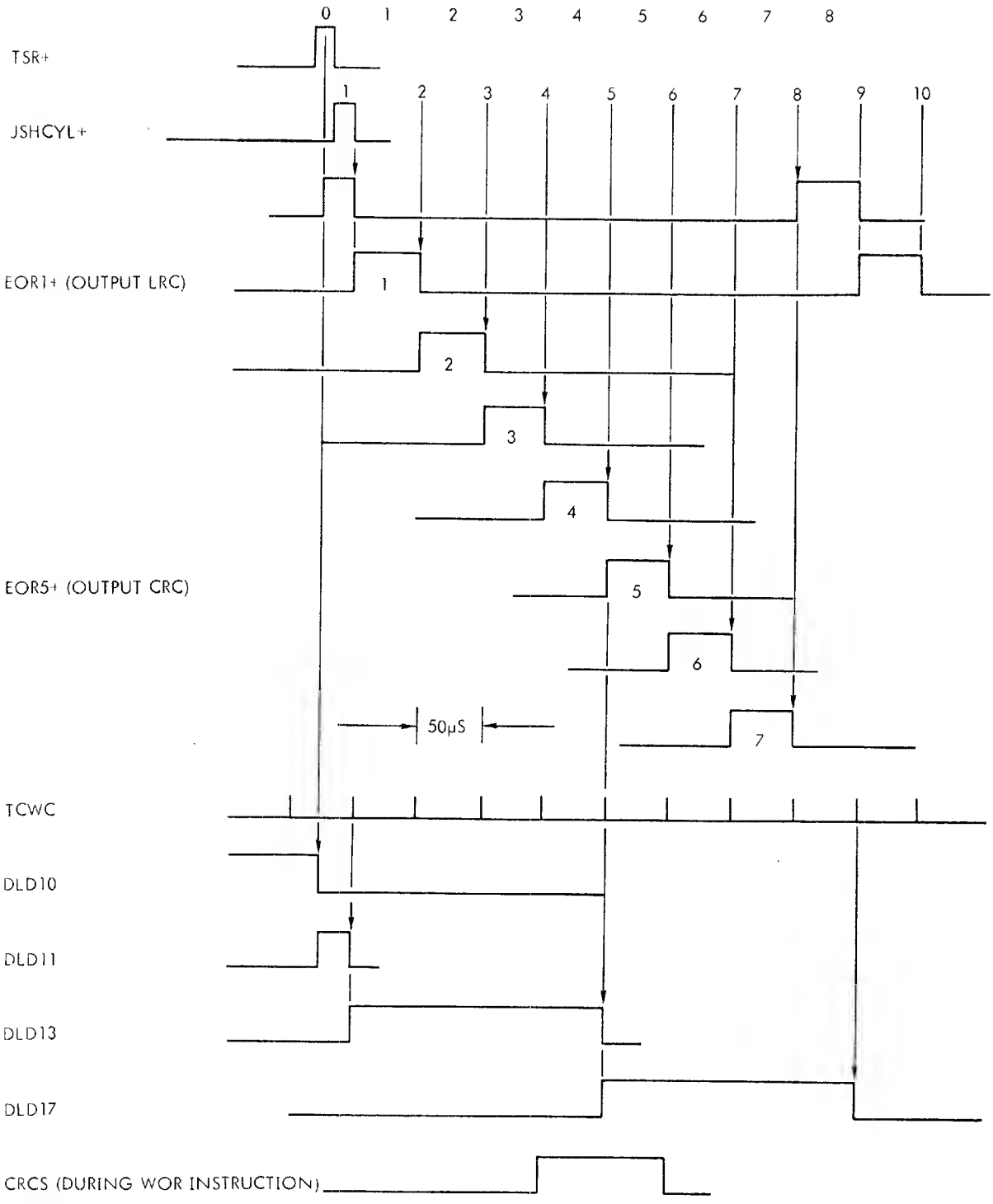
VTI2-132

Write-One-Record Timing



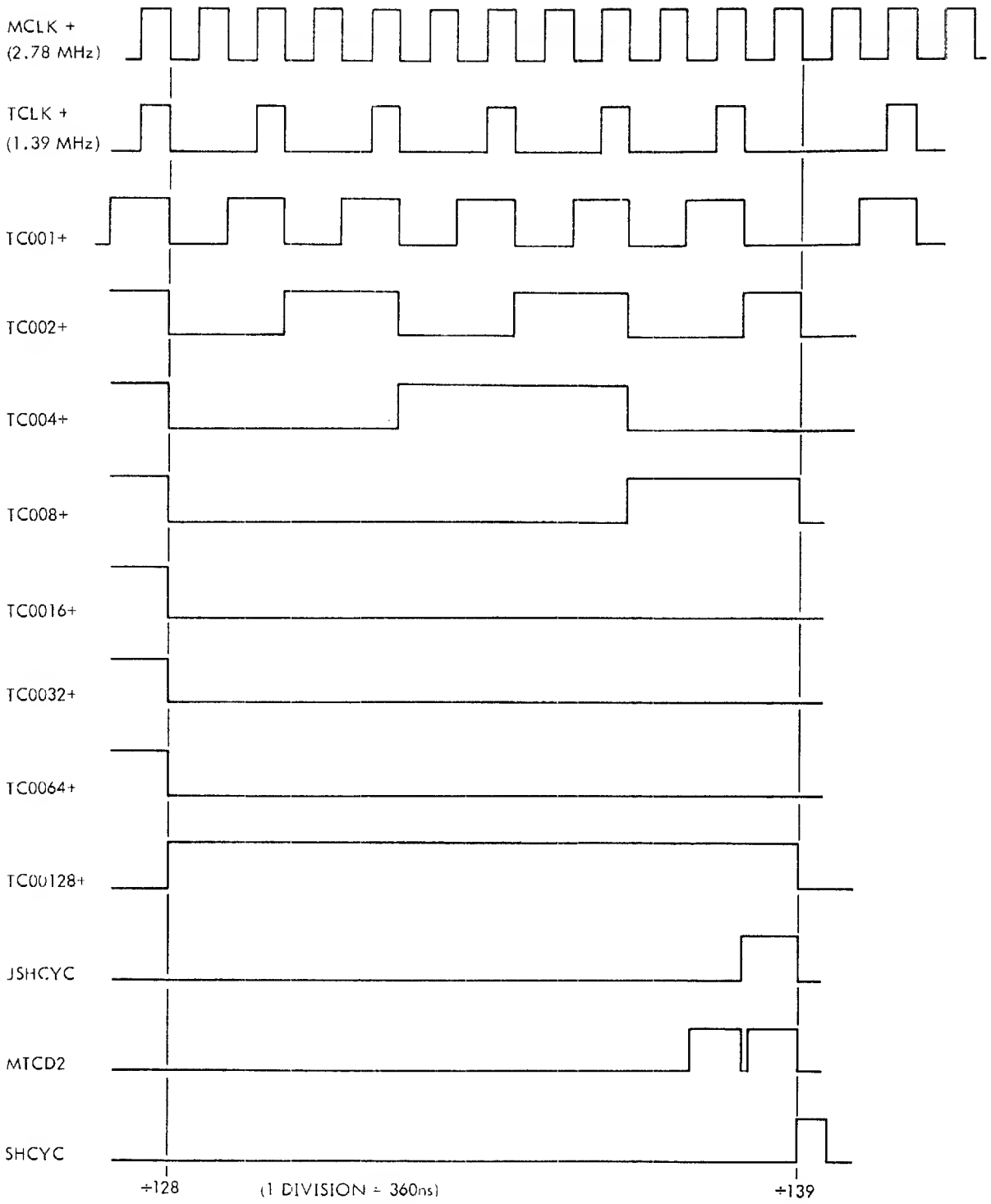
VTI2-133

Clock Timing-Write



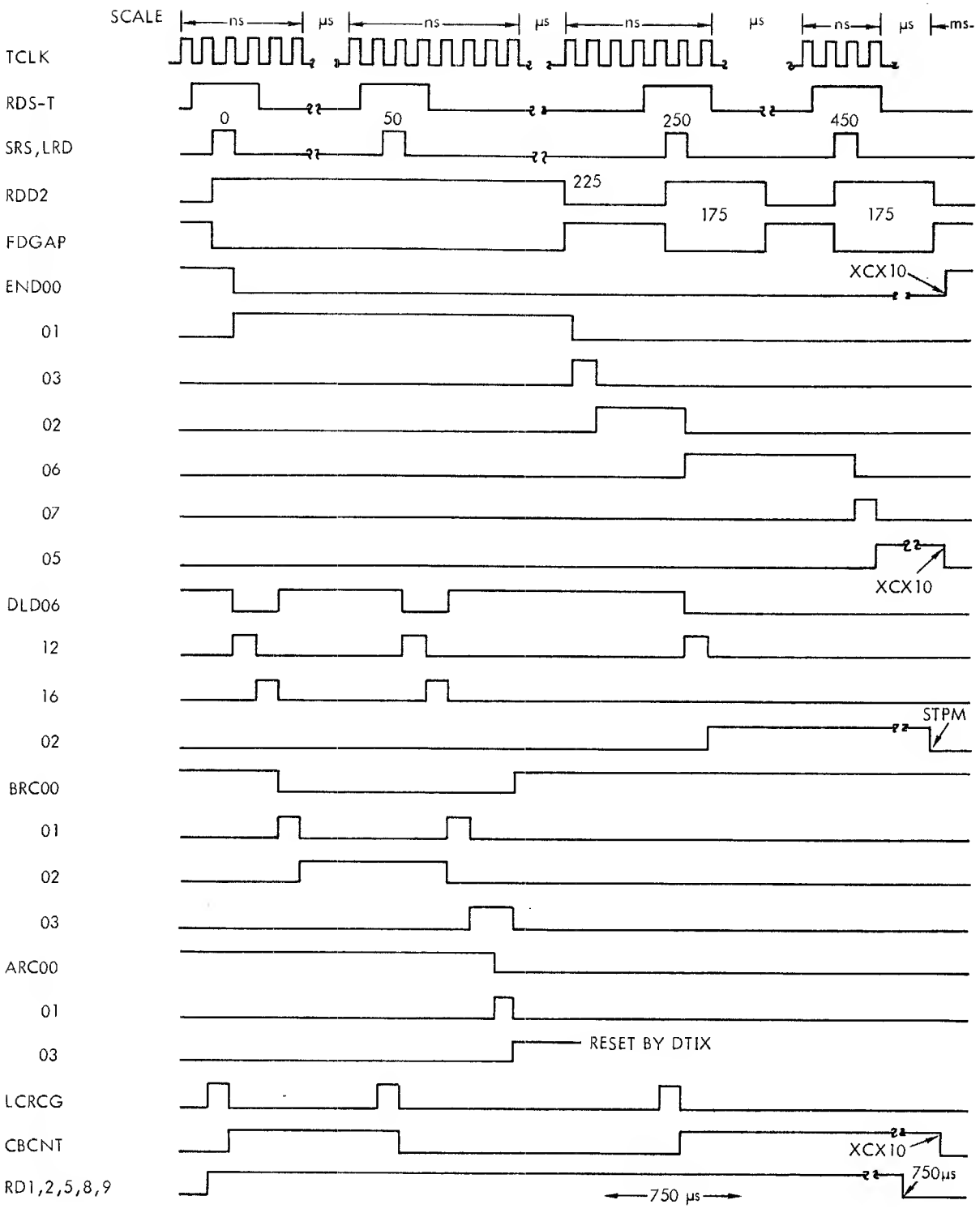
VTI2-129

Data Control Timing



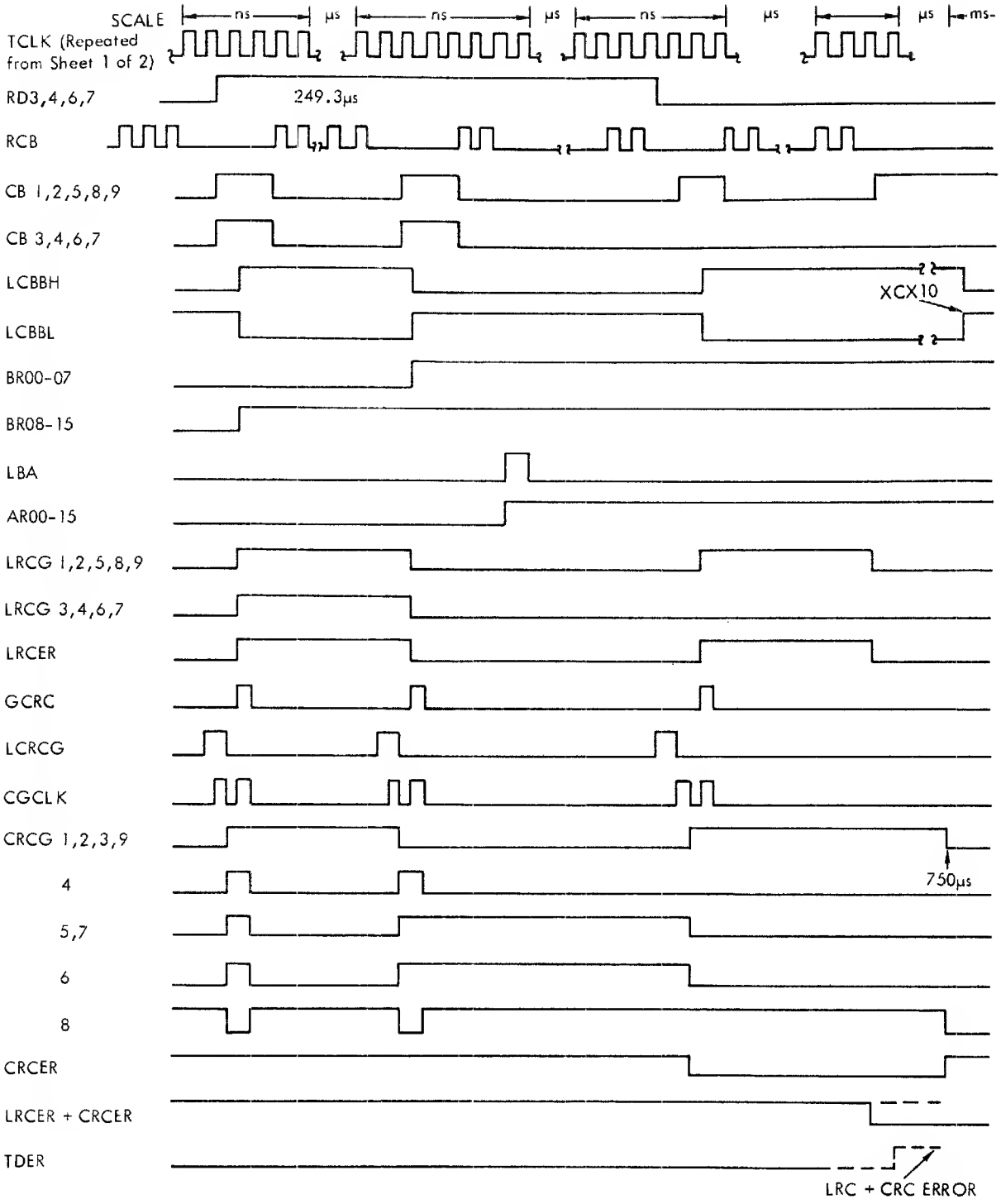
VTI2-130

Master Clock Timing



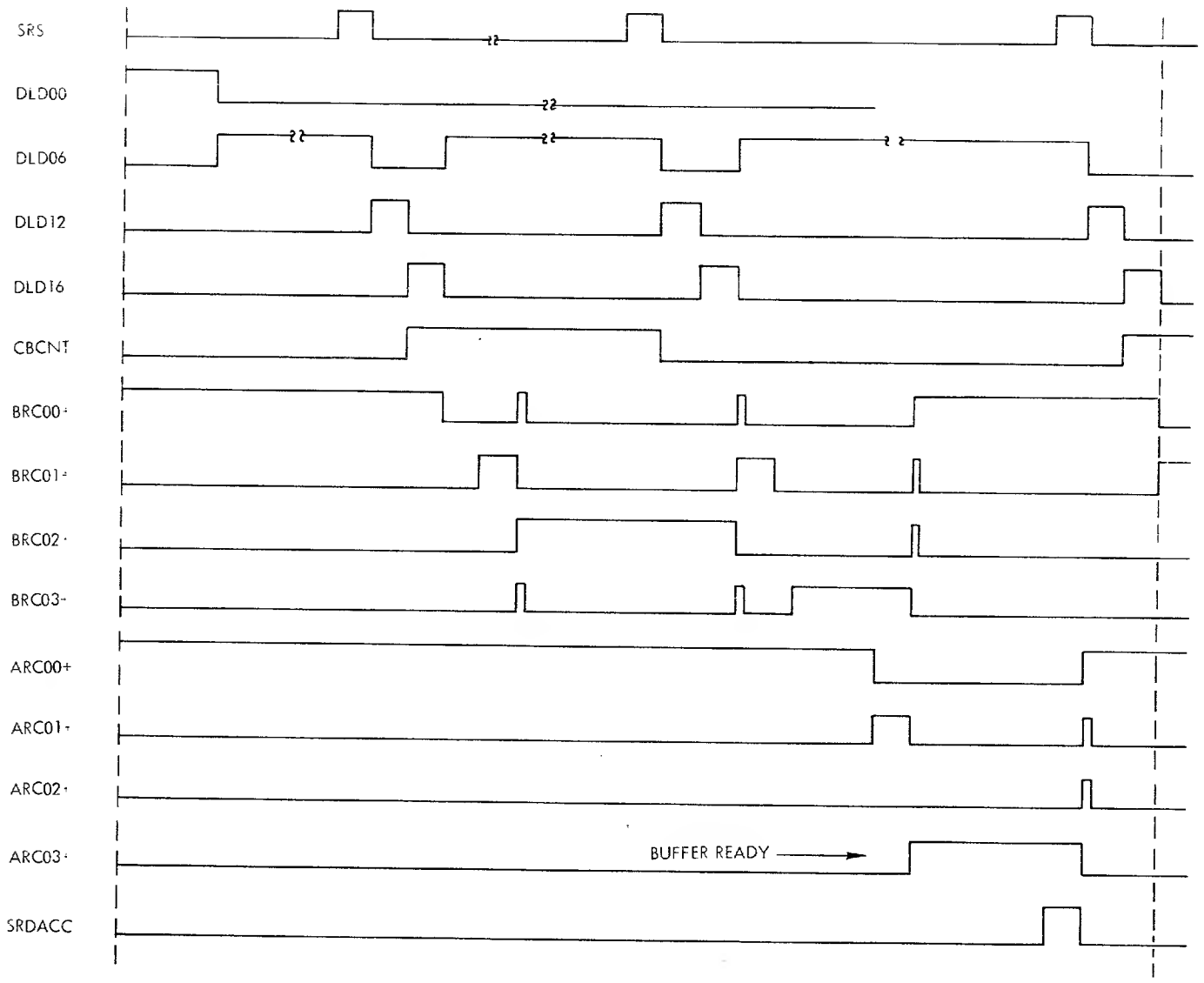
VTI2-135

MTC Test Program: Read-One Record (Sheet 1 of 2)



VTI2-136

MTC Test Program: Read-One Record (Sheet 2 of 2)



VT12-J34

Read-One-Record Timing